MICE Tracker Electronics

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Terry Hart,
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Quick AFE II t Overview

- AFE II t boards are second generation D0 Analog Front End tracker boards capable of digitizing input charges and times being developed for D0 DAQ upgrade.

- 16 AFE II t boards will read out data from 2 MICE scintillating fiber trackers.
Fermilab and RAL AFE II t Test Stands

• MICE IIT group will
  – Help D0 test ~350 AFE II t boards with MICE using 16 boards + spares
    • IIT summer students Ben Freemire and Michael Wojcik will assist with testing
  – Develop MICE-specific firmware to optimize event readout
    • IIT engineer Bill Luebke and I are working on this.

• RAL group will
  – Perform firmware diagnostic work
    • RAL engineers Craig MacWaters and Senerath Galagedera and IIT group discussing particular tasks and tests for boards
AFE II t Board Testing Schedule

• Test stand progress
  – Test stands at Fermilab set up, and IIT group has been practicing going through preliminary versions of tests.
  – Test stand at RAL almost ready.

• Testing procedures being worked out by D0 project engineers Paul Rubinov, Kwame Bowie and Tom Fitzpatrick with assistance from IIT group.
  – Inspection and Mechanical Assembly
  – Programming and Bench Top
  – Calibration and Testing
  – Burn in at Combined Test Stand
  – Repair and Debug
AFE II t Board Testing (cont.)

- First boards expected this week. After this week, about 40 – 50 boards/week will arrive.

- Ben, Mike, Bill, and I have been instructed on handling and testing boards.

- Board throughput should be about 4/week so that all should be tested by late August/early September.
Firmware Development, Current Capability and Goal

• Current capability of ~225 muons/ms due to 113 ns digitization time for all channels, even those below threshold.
  – Digitization process requires about 100 ns per channel due to digitization rise and fall times.

• Overall data throughput goal: Charge and time digitization of 600 muons/ms.
  – Motivation: worst-case scenario of RF noise being much larger than expected. Noise hits would need to be rejected by using total charge and timing information.
  – If RF noise rate is low as expected, then MICE can use discriminator hit map to reconstruct muon trajectories.
Firmware Development, Plan for Increasing Data Throughput

- IIT group is studying AFE II firmware and schematic drawings with D0 and RAL engineers to devise way to use
  - 2 clock cycles to skip channels below threshold (~40 ns)
  - 5 or 6 clock cycles to digitize channels above threshold (~100 ns)

- Firmware modifications will alter
  - Analog Field Programmable Gate Array (AFPGA) control of charge and time digitization.
  - Transfer of digitized data to VME LVDS Serdes Buffer (VLSB) banks.
Tracker Electronics Schedule and Outlook

- Full scale AFE II board testing starting with completion scheduled for late August/early September.

- Firmware development to increase muon event data throughput underway with initial revised firmware expected in a couple months.